IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: H. MATSUOKA et al

Serial No. 09/592,648 Filed: June 13, 2000

Group Art:

2814

Examiner:

D. Nguyen

For:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

AND A METHOD OF MANUFACTURE THEREOF

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

July 31, 2003

Sir:

In accordance with the duty of disclosure, the Applicants inform the Examiner of the documents cited during prosecution of the parent application, USSN 09/592,648.

The Applicants request the Examiner to initial and return a copy of the attached PTO-1449 form as an indication that the references have been considered.

Respectfully submitted,

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Date: July 31, 2003

FORM PTO-1449 (REV. 7-80)			U.S. DEPART PATENT AND	MENT OF COMMERC TRADEMARK OFFICE					
LIST OF DOCUMENTS CITED BY APPLICANT					APPLICANT				
(Use several sheets if ned					H. MATSUOKA et a	GROUF	· · · · · · · · · · · · · · · · · · ·		
				07/31/03	2814				
				U.S. PATEN	NT DOCUMENTS				
* EXAMINER INITIAL		DOCUMENT	DATE		NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate	
	AA	6,130,449	10/2000	Matsuoka et	al				
	АВ	6,100,117	08/2000	Hao et al					
	AC								
	AD								
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				FOREIGN PAT	ENT DOCUMENTS				
		DOCUMENT	DATE	COUNTRY		CLASS	SUBCLASS	TRANS YES	NO NO
	AL	07-066299	03/10/95	Japan					
	АМ		_						
	AN								
	AO								
	AP								
			OTHER DOCU	MENTS (Including A	Author, Title, Date, Pertinent	Pages, etc.)			
AF	AR	Ahn et al "Bidirectional Matched Global Bit Line Scheme for High Density							
		DRAMs", Symposium on VLSI Circuits, 1993, pp. 91-92.							
	AS								
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-v.			- <u>-</u>		Ta Jan Walington				
EXAMINER					DATE CONSIDERED				
* EXAMINE	R: Initi	al if reference consider	ed, whether or not citati	on is in conformance with MP	EP 609; Draw line through citation if not in	n conformance and not	considered. Includ	e copy of th	is form